EUROPEAN PATENT APPLICATION

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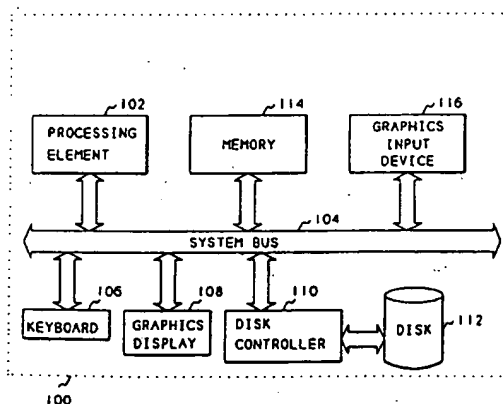(72) Inventor: Juran, Michael T.
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(54) Common symbol library architecture.

(57) Disclosed is a schematic capture and design verification system wherein the graphic symbol (402) linked to a component is separated from the model (422, 426) used to simulate the component. Each component has a graphics symbol (402) linked to a link or scion page (404). The link page (404) also contains a list of all models that can be used with the component. The system allows a model to be selected (406) for each component in a schematic, and allows the model to be changed at any time. The system also allows the models for all compo-nents to be changed with a single command. The user enters a schematic (602) into the system, then selects a model for each component used in the schematic. After a model has been selected for each component, the user requests the system to build a netlist that describes the schematic to a simulator or other analysis or synthesis tool. In building the netlist (616), parameters are extracted from the link page for each component and included in the netlist to be used by the simulator. When a different simulation is desired by the user, the user instructs the system to change the model linked to the components to a new model suitable to the second simulator. The system then builds a new netlist, using parameters specific to the new model and the second simulator.

FIG. 1

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	IEEE INTERNATIONAL CONFERENCE ON CIRCUITS AND COMPUTERS SEPTEMBER 28 - OCTOBER 1 1982 NEW YORK US pages 503 - 506 KAWAMOTO 'schematic entry system with a query feature' * page 504, column 2, line 35 - line 40 * * page 505, column 2, line 1 - line 16 * * page 506, column 1, line 5 - line 10; figures 3,7 *	1,2,5,6, 11	G06F15/60
A	ELECTRONIC DESIGN. vol. 35, no. 5, March 1987, HASBROUCK HEIGHTS, NEW JERSEY US pages 96 - 102 BENEDICT ET AL 'versatile schematic capture set caters to custom - IC designers' * page 97, column 1, line 36 - line 43; figure 2 *	1,2,5,6, 11	
A	EDN ELECTRICAL DESIGN NEWS vol. 32, no. 3, 5 February 1987, NEWTON, MASSACHUSETTS US pages 175 - 184 WATERS ET AL 'use an interchange format to port component libraries' * page 176, column 1, line 26 - page 177, column 2, line 11 *	1,2,5,6, 11	TECHNICAL FIELDS SEARCHED (Int. Cl.5) G06F
A	EP-A-0 196 940 (FAIRCHILD SEMICONDUCTOR CORPORATION) 8 October 1986		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 MARCH 1993	GUINGALE A.

EPO FORM 1503 03.82 (P0401)